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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,434	09/05/2003	Hitoshi Yamamoto	2271/70977	8466

7590 04/11/2005

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,434	YAMAMOTO, HITOSHI	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2 and 10 to 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2 and 10 to 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/656434 Attorney's Docket #: 2271/70977
Filing Date: 9/5/2003; claimed foreign priority to 9/6/2002

Applicant: Yamamoto

Examiner: Alexander Williams

Applicant's Amendment filed 1/21/05 to the Applicant's election of Group I (claims 1 and 2), filed 7/15/2004, has been acknowledged.

Claims 3-9 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2 and 10 to 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Aklyama et al. (U.S. Patent # 6,853,063 B2).

As to claim 1, similar claim 10 and there dependent claims, Aklyama et al. (figures 1 to 11) specifically figures 1A and 1B show a semiconductor device which integrates a plurality of semiconductor chips **210,220** into a single package, comprising: a first semiconductor chip **210** which includes a plurality of first bonding pads **(inherit)** outputting first signals having a first level; and a second semiconductor chip **220** which includes a plurality of second bonding pads **(inherit)** electrically coupled to a part of the plurality of first bonding pads to receive the first signals having the first level from the first semiconductor chip through the part of the plurality of-first bonding pads and a

plurality of third bonding pads **(inherit);** and a signal level conversion circuit **(converter)**, wherein said signal level conversion circuit converts the first signals received through the plurality of second bonding pad into second signals having a second level different from the first level and outputs the second signals through the plurality of third bonding pads.

(23) (Embodiment 5)

(24) This embodiment is such that the semiconductor device of from the embodiment 1 to embodiment 4 is applied to an analog front end (AFE). A circuit configuration of this embodiment is shown in FIG. 7 in block form. In FIG. 7, reference numeral 1000 designates the semiconductor device of from the embodiment 1 to embodiment 4.

(25) The first chip 10's primary side circuit 210 is mainly formed of a two-line/four-line conversion circuit, multiplexer (MUX), analog-to-digital converter (ADC) circuit, digital-analog converter (DAC) circuit, pre-filter, post-filter, control circuit for performing reset and power-down operations, and reference voltage generation circuit. The reference voltage generator circuit is operable to generate a reference voltage Vref to be supplied to analog circuitry operatively associated therewith.

(26) The secondary side circuit 220 of second chip 20 consists essentially of a control circuit operable to perform digital signal processing, input/output control, reset and powerdown operations. Here, its digital signal processing and input/output control circuit section is typically made up from a DA conversion input buffer, AD conversion output buffer, built-in or "internal" digital signal processor (DSP), DSP input/output transfer controller, received signal/data buffer and transmit data buffer, although not specifically depicted herein.

(27) An explanation will now be given of an operation of the internal circuitry of the semiconductor device 1000. The 2-line/4-line converter circuit is the circuitry that performs changeover or switching of 2-line circuit lines being connected

to LINE+, LINE- to a 4-line circuit within the semiconductor device 1000 in a way conformity with occurrence of signal transmit and receive events in cases where the semiconductor device 1000 is for use in modulator/demodulator or "modem" devices, which circuit functions as a line impedance matching and input/output amplifier.

(28) In the signal receipt system, one or more analog input signals are input and output via the 2-line/4-line converter circuit or, alternatively, input from IN+, IN- terminals, wherein this changeover is done by the multiplexer MUX. The analog input signals are such that signals of unnecessary frequency bands are deleted therefrom by the prefilter (e.g. second-order low-pass filter with its cutoff frequency of 48 KHz) prior to execution of AD conversion. And a second-order .DELTA..SIGMA. modulator ADC operable at 2 Msps is used to output a 2-bit digital signal once at a time whenever a time of 0.5 .mu.s is elapsed, which is then processed to decrease in pulse number or "thinned out" into 32 Ksps at a decimeter of the next stage (not shown); thereafter, 16-bit/w data is subject to serial conversion to 2 Msps prior to entering the isolator circuit. The data passed through such isolator circuit will then be input to the digital signal processing and input/output control circuit. Here, flat characteristic correction and/or low-pass filter processing at 4 KHz or less is performed causing it to be transferred toward an external DSP 600 as 16-bit/w data per 8 Ksps (i.e. input to RXD terminal).

(29) Next, in the signal transmit system, data being output from a TDX terminal of the external DSP 600 will then be subject to similar processing to that executed in the signal receipt event at the digital signal processing and input/output control circuit. 16-bit/w data is serial-converted into 2 Msps before entering the isolator circuit and, after having passed through the isolator circuit 100, enters an interpolation filter (not shown). The resultant data that has been interpolation-processed and thus becomes 6-bit/w data is then converted by a .DELTA..SIGMA. modulator DAC into a corresponding analog signal. After having removed at the postfilter certain turnaround or "folded" components presently residing through the interpolation processing or the like, the signal is output via the 2-line/4-line converter circuit onto 2-line circuit lines being connected to LINE+, LINE-.

(30) It must be noted that the operation timing of internal circuitry of the semiconductor device 1000 is determined with certain clocks being each used as the reference therefor, which clocks include a clock of 2 MHz (MCLK) as given by the external DSP 600 and a clock as converted therefrom at a phase-locked loop (PLL) present within the control circuit of the secondary side circuit 220 to have a frequency of 16 MHz which is eight times greater than that of the former. These reference clock signals are also sent to the control circuit of the primary side circuit 210 via the isolator circuit 100, based on which signals a variety of timing control operations are being performed.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2 and 10 to 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawaya (U.S. Patent # 5,245,215) I view of Sakuma et al. (U.S. Patent Application Publication # 2003/0001808 A1).

As to claim 1, similar claim 10 and there dependent claims, Sawaya (figures 1A to 15B) specifically figures 1A and 1B show a semiconductor device which integrates a plurality of semiconductor chips **12-1,12-2** into a single package, comprising: a first semiconductor chip **12-2** which includes a plurality of first bonding pads **17** outputting first signals having a first level; and a second semiconductor chip **12-1** which includes a plurality of second bonding pads **17** electrically coupled to a part of the plurality of first bonding pads to receive the first signals having the first level from the first semiconductor chip through the part of the plurality of-first bonding pads and a plurality of third bonding pads **17** which converts the first signals received through the plurality of second bonding pad into second signals having a second level different from the first level and outputs the second signals through the plurality of third bonding pads. Sawaya show the structure and features of the claimed invention as detailed above, but fail to explicitly show a signal level conversion circuit, wherein the signal level conversion circuit converts the first signals into second signals having a second level different form the first level and outputs the second signals. Since this language is functional limitation that must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art, consideration of function language is acceptable so long as it sets definite boundaries on the patent protection sought. *(See MPEP 2173.05g) In re Bar, 170 USPQ 33 (CCPA 1971).* In consideration of the functional limitations for purpose of applying the prior art, the Examiner, applied the prior art with features of the apparatus structurally, and did not distinguish from the prior art in terms of structure rather than function alone.

(see MPEP 2114) See In re Swinehart, 169 USPQ 226 (CCPA 1971); In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997). The Examiner has a reason to believe that the function limitation can be performed by the prior art structure using any given amplifier the structure. The recitation directed to the manner in which a claims apparatus is intended to be used does not distinguish the claimed apparatus form the prior art if the prior art has the capability to so perform. *(See MPEP 2114 and Ex parte Masham, 2 USPQ2d 1647 (1987))* However, Sawaya show the claimed structure of the claimed device. The claimed language referring to the signal level conversion circuit recited the function of the claimed semiconductor chip. Sawaya's semiconductor chip products a signal level. Any device structure can have the level or amplitude signal changed to a desired output level in a signal circuit system with a signal conversion circuit or an amplifier as desired to increase the output signal or volume of a signal. It would be obvious to one of ordinary skill in the art to use any means of signal level conversion circuit or amplifier to make the signal output different from the input signal.

Nevertheless, Sakuma et al. is cited for showing a liquid crystal display. Specifically, Sakuma et al. (figures 1 to 21) specifically figures 1 and 2 discloses a package, comprising: a first semiconductor chip **20** having a first level; and a second semiconductor chip **20** to receive the first signals having the first level from the first chip; and a signal level conversion circuit **25**, wherein the signal level conversion circuit converts the first signals received it into the second signals having a second level different from the first level and outputs the second signal for the purpose of providing a

display diver for the purpose of measuring the potential difference on a power supply line.

DOCUMENT-IDENTIFIER: US 20030001808 A1

Summary of Invention Paragraph - BSTX (5):
[0004] In general, when an image is displayed on a liquid crystal display (LCD), image signals are output from a graphics controller in a system unit or system part of a PC or the like (i.e., host's side) via a video interface. An LCD controller LSI, which receives these image signals, supplies signals to each IC in a source driver (i.e., X driver, LCD source driver) and gate driver (i.e., Y driver), and then a voltage is applied to each source electrode and each gate electrode in a TFT array arranged in a matrix fashion, thereby leading to displaying images. As a mounting and wiring scheme employed in this LCD source driver, technologies called chip-on-glass (COG) and wiring-on-array (WOA) have recently become the focus of attention. Also, a technology is being developed where a driver LSI is arranged in a TCP (tape carrier package) and connected to the TFT array substrate (glass substrate) via the TCP. It is expected that manufactures' costs will be greatly reduced by applying these technologies to attach ICs directly on the glass substrate or via the TCP as well as to eliminate wiring on a printed circuit board.

Detail Description Paragraph - DETX (8):
[0046] FIG. 2 depicts a configuration of source driver IC 20 according to the present invention. Source driver IC 20 comprises an interface circuit 30 indicative of the features of the invention, and a control circuit 21 that receives video signals and outputs from interface circuit 30 and controls outputs to liquid crystal cells 2 constituting the TFT array. Furthermore, there are provided a shift register 22 operating according to the output from control circuit 21, a two-stage data latch 23, and a buffer amplifier 25 as well as a digital-to-analog (D/A) converter 24 that receives a gamma correction voltage and D/A converts the value of data latch 23 to output to buffer amplifier 25.

2. The semiconductor device as defined in Claim 1, the combination with Sawaya show wherein the second level is greater than the first level.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Sakuma et al.'s signal level conversion circuit to modify Sawaya's single package for the purpose of providing a display diver for the purpose of measuring the potential difference on a power supply line.

Response

Applicant's arguments filed 1/21/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that Sawaya is not directed at the problem that some chips operate at one level while other chips operate at a second level which is different from the first level, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

The insertion of Applicant's additional claimed language, for example, "in claim1 and new claims 10-15" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any signal can be amplified in a circuit device.

Field of Search	Date
U.S. Class and subclass: 257/685,723,666,777,686,728,676,678,787,784,786,696,	9/14/04 4/7/05

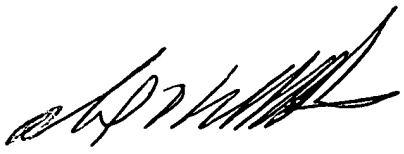
698,691,690	
Other Documentation: foreign patents and literature in 257/685,723,666,777,686,728,676,678,787,784,786,696, 698,691,690	9/14/04 4/7/05
Electronic data base(s): U.S. Patents EAST	9/14/04 4/7/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
4/7/05



Primary Patent Examiner
Alexander O. Williams